Productivity in metrology

KLA-Tencor has introduced Archer AIM+, its latest overlay metrology solution to address chipmakers' lithography overlay control needs beyond the 65nm node.

Archer AIM+ drops total measurement uncertainty (TMU) by 50% and increases throughput by up to 20%, compared to KLA-Tencor's previous Archer AIM system.

Archer AIM+ is currently being evaluated by memory and logic device manufacturers and chosen by several leading-edge fabs.

Archer AIM+ uses KLA-Tencor's grating-style targets, which are more robust to chemical mechanical planarisation processing than box-in-box targets, having less open area for CMP processing to cause target degradation.

AIM targets are also denser than traditional box-in-box targets, collecting more information for improved correlation to in-device overlay performance.

For customers wanting traditional box-style targets, KLA-Tencor also offers box-in-box compatible Archer XT+.

Archer AIM+ offers a new optic system design and improved illumination. This cuts TMU to within 2.1nm, bettering the 45-nm node overlay control outlined in the 2004 ITR for Semiconductors.

New software algorithms have been added for high-precision measurements on low contrast and post-CMP layers, which are particularly difficult to measure by traditional overlay control techniques.

Contact: www.kla-tencor.com

Cell for data

IBM makes interesting partnerships. One with Mercury Computer Systems Inc will see the Cell microprocessor technology built into new systems for data-intensive uses.

Mercury is the first outside the gaming industry to use Cell micro technology design services from IBM. Mercury has initial plans to integrate the Cell microprocessor technology into a wide variety of future products, with the aim of boosting performance for its customer applications.

New sensor capabilities in these markets are dramatically increasing the volumes of available data to be processed. The optimised Cell products will be targeted at current and new applications in medical imaging, industrial inspection, aerospace & defence, seismic processing and telecommunications.

Silicon at 105GHz

UMC has fabricated a Voltage-Controlled Oscillator (VCO) with a record-setting fundamental operating frequency of 105GHz using its 0.13µm RF CMOS process technology. The chip was developed by Silicon Microwave Integrated Circuits and Systems Research Group, Electrical & Computer Engineering at the University of Florida, Gainesville.

The highest recorded fundamental operating frequency for CMOS circuits was a 103-GHz oscillator fabricated using a 90nm CMOS process that consumed four time the power. The new effort by the University was 105-GHz VCO and a second 99-GHz VCO with a tuning range of 2.4GHz, using the 0.13µm process.

The effort signifies that VCOs for 94GHz industrial, scientific medical band and imaging as well as 60GHz WLAN and 77GHz radar applications can be implemented using UMC's process. VCOs are in virtually all RF and wireless systems.

"UMC continues to provide the advanced process technologies that are used to power today's highest-performance applications," said Patrick T Lin, chief system architect at UMC.

"Developing ICs of this calibre in 0.13µm CMOS is a huge milestone," said Florida University's Professor Kenneth O. "If we incorporate frequency doubling techniques, we should be able to generate signals with 200 Ghz frequencies and higher.

"This has the potential to open up far-infrared to CMOS. UMC's role in our development was pivotal as this foundry provided the process and parameters that brought the chip to silicon quickly and easily."

Source:www.ee.ucla.edu

IBM goes low-power ASICs

IBM is to move to 65nm ASIC offerings, with its first comprehensive low-power ASIC, moving into consumer electronics and digital media markets that need low-power functionality for mobile and handheld devices. "This is very much a strong statement of IBM's pursuit of the low-power marketplace and, specifically, going after the very high growth in consumer electronics," says Richard Busch, director of IBM ASIC products.

The low-power 65nm ASIC offering, Cu-65LP, has leakage currents reduced some 30 times from the previous 90nm ASICs and performance is increased by up to 20%. Both 65nm ASICs, the low-power Cu-65LP and a high-performance Cu-65HP detailed at the 2005 Design Automation Conference, can fit nearly twice as many circuits on a die compared with the equivalent 90nm ASIC.

"We've got a very strong and prominent position, historically, as an ASIC provider," said Busch. "We're basically taking all the knowledge and learning that we have garnered from our own systems experience and participation in the other segments and moving to expand very aggressively in this area."

The chips use strained silicon and statistical techniques for timing and optimisation. They also provide power management features that include voltage Island technique controls power, a multiple threshold voltage library, and integrated noise, power and timing methodology allowed first pass success designs.

The offering includes standard-cell logic design libraries; multiple I/O families; embedded SRAM and DRAM; a collection of cores, including industry leading high-speed SerDes and embedded microprocessors highlighting PowerPC architecture; and a wide range of packaging solutions.

The low-power ASIC is built with ARM/Artisan libraries. ARM is co-developing 65nm low-power libraries and selected cores with IBM. The Cu-65LP design kit is available this quarter, followed by the high-performance design kit later in the year. Volume production for the Cu-65 low power and high performance offerings will begin respectively in Q1 and Q3 of 2007.